

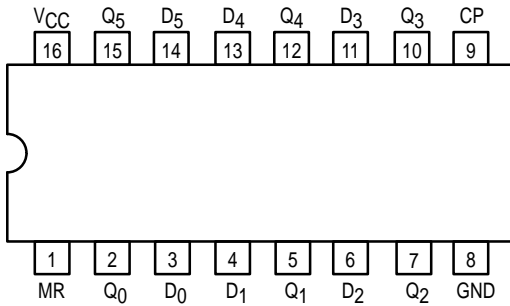


# HEX D FLIP-FLOP

The LSTTL/MSI SN54/74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Asynchronous Common Reset
- Input Clamp Diodes Limit High Speed Termination Effects

### CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

- D<sub>0</sub>–D<sub>5</sub> Data Inputs
- CP Clock (Active HIGH Going Edge) Input
- MR Master Reset (Active LOW) Input
- Q<sub>0</sub>–Q<sub>5</sub> Outputs (Note b)

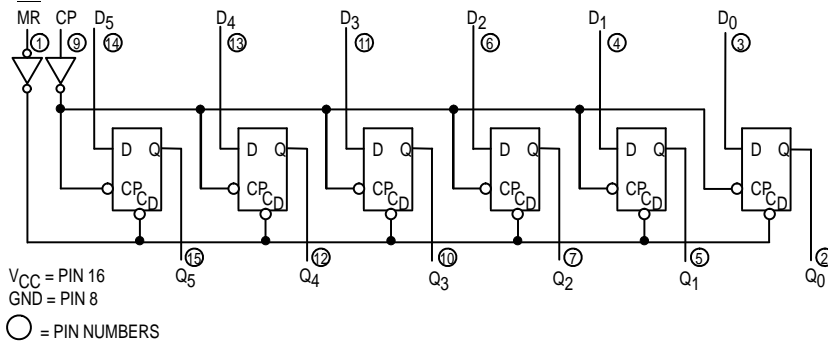
### LOADING (Note a)

| HIGH     | LOW          |
|----------|--------------|
| 0.5 U.L. | 0.25 U.L.    |
| 0.5 U.L. | 0.25 U.L.    |
| 0.5 U.L. | 0.25 U.L.    |
| 10 U.L.  | 5 (2.5) U.L. |

### NOTES:

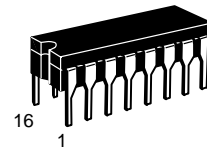
- a. 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

### LOGIC DIAGRAM

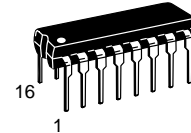


# SN54/74LS174

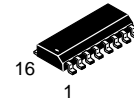
## HEX D FLIP-FLOP LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

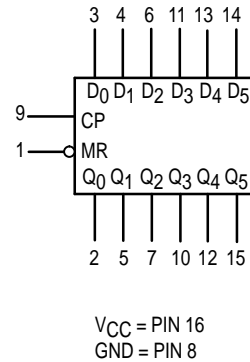


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

### LOGIC SYMBOL



# SN54/74LS174

## FUNCTIONAL DESCRIPTION

The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ( $\overline{\text{MR}}$ ) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## TRUTH TABLE

| Inputs (t = n, MR = H) | Outputs (t = n+1) Note 1 |
|------------------------|--------------------------|
| D                      | Q                        |
| H                      | H                        |
| L                      | L                        |

Note 1: t = n + 1 indicates conditions after next clock.

## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | -55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | -0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                      | Limits |       |      | Unit | Test Conditions  |   |
|-----------------|--------------------------------|--------|-------|------|------|--|---|
|                 |                                | Min    | Typ   | Max  |      |  |   |
| V <sub>IH</sub> | Input HIGH Voltage             | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs   |   |
| V <sub>IL</sub> | Input LOW Voltage              | 54     |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs  |   |
|                 |                                | 74     |       | 0.8  |      |  |   |
| V <sub>IK</sub> | Input Clamp Diode Voltage      |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA  |   |
| V <sub>OH</sub> | Output HIGH Voltage            | 54     | 2.5   | 3.5  | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table |   |
|                 |                                | 74     | 2.7   | 3.5  | V    |  |   |
| V <sub>OL</sub> | Output LOW Voltage             | 54, 74 |       | 0.25 | 0.4  | I <sub>OL</sub> = 4.0 mA   | V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table |
|                 |                                | 74     |       | 0.35 | 0.5  | I <sub>OL</sub> = 8.0 mA   |   |
| I <sub>IH</sub> | Input HIGH Current             |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V   |   |
|                 |                                |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V   |   |
| I <sub>IL</sub> | Input LOW Current              |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V   |   |
| I <sub>OS</sub> | Short Circuit Current (Note 1) | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX  |   |
| I <sub>CC</sub> | Power Supply Current           |        |       | 26   | mA   | V <sub>CC</sub> = MAX  |   |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN54/74LS174

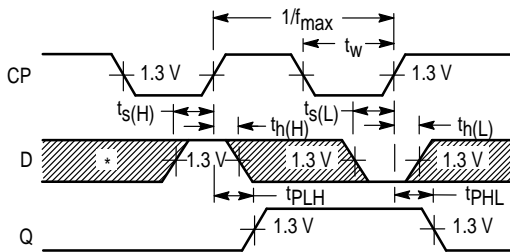
## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

| Symbol                               | Parameter                          | Limits |          |          | Unit | Test Conditions                                   |
|--------------------------------------|------------------------------------|--------|----------|----------|------|---|
|                                      |                                    | Min    | Typ      | Max      |      |   |
| f <sub>MAX</sub>                     | Maximum Input Clock Frequency      | 30     | 40       |          | MHz  | V <sub>CC</sub> = 5.0 V<br>C <sub>L</sub> = 15 pF |
| t <sub>PHL</sub>                     | Propagation Delay, MR to Output    |        | 23       | 35       | ns   |   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay, Clock to Output |        | 20<br>21 | 30<br>30 | ns   |   |

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

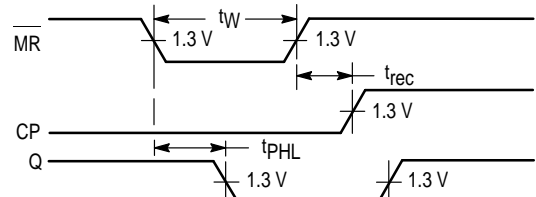
| Symbol           | Parameter               | Limits |     |     | Unit | Test Conditions         |
|------------------|-------------------------|--------|-----|-----|------|-------------------------|
|                  |                         | Min    | Typ | Max |      |                         |
| t <sub>W</sub>   | Clock or MR Pulse Width | 20     |     |     | ns   | V <sub>CC</sub> = 5.0 V |
| t <sub>s</sub>   | Data Setup Time         | 20     |     |     | ns   |                         |
| t <sub>h</sub>   | Data Hold Time          | 5.0    |     |     | ns   |                         |
| t <sub>rec</sub> | Recovery Time           | 25     |     |     | ns   |                         |

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

## DEFINITIONS OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recog-

niton. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.